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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/749,943	12/31/2003	John C. Rudelic	INTEL22	6666

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TROUTMAN SANDERS LLP
600 PEACHTREE STREET , NE
ATLANTA, GA 30308

EXAMINER	
CHANG, ERIC	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 12/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/749,943	RUDELIC, JOHN C.	
	Examiner	Art Unit	
	Eric Chang	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 September 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 September 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-21 are pending.

Claim Rejections - 35 USC § 103

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

3. Claims 1, 8 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,793,694 to Akiba et al., in view of Applicant's Admitted Prior Art.

4. As to claim 1, Akiba discloses a system comprising a first memory [42a] and a second memory [42b]; a pulse generator [86] operable to generate a first current draw waveform of current to the first memory and a second current draw waveform of current to the second memory [col. 1, lines 61-67, col. 2, lines 1-16, and col. 6, lines 42-55]; and a delay circuit [88] operable to inject a time delay between the first and second current draw waveform of current [col. 6, lines 35-55], wherein the time delay is less than a duration of the current draw waveform applied to the first memory [FIG. 14]. Akiba teaches that the activation of SAE driver causes a first current draw to be directed to the first memory, and a second current draw to be directed to the first memory, via their respective components, including sense amplifiers. Akiba further teaches that the activation of the second memory is delayed, thereby causing a delay between the first and second currents being drawn.

Akiba teaches the limitations of the claim, including a first and second memory, but does not teach that the pulse generator is coupled to a first write state machine a second write state machine.

Applicant's Admitted Prior Art teaches an electronic system having a plurality of memories [paragraph 2]. Thus, Applicant's Admitted Prior Art teaches an electronic system with a first and second memory configuration similar to that of Akiba. Applicant's Admitted Prior Art further teaches that each memory has a controller comprising a write state machine [paragraph 2].

At the time that the invention was made, it would have been obvious to a person of ordinary skill in the art to employ the write state machines as taught by Applicant's Admitted Prior Art. One of ordinary skill in the art would have been motivated to do so that the memories would receive the proper amount of current.

It would have been obvious to one of ordinary skill in the art to combine the teachings of the cited references because they are both directed to the problem of initializing power to a plurality of memories in an electronic system. Moreover, the write state machines taught by Applicant's Admitted Prior Art would improve the functionality of Akiba because it allowed for performing erase and program operations [paragraph 2].

5. As to claim 8, Akiba discloses a method comprising applying a first pulse of current to a first memory and a second pulse of current to a second memory [col. 6, lines 35-55]; and injecting a time delay between the first and second pulse of current [col. 6, lines 35-55].

Applicant's Admitted Prior Art further teaches that each memory has a controller comprising a write state machine [paragraph 2].

6. As to claim 15, Akiba discloses a computer readable medium having instructions comprising: applying a first pulse of current to a first memory and a second pulse of current to a second memory [col. 6, lines 35-55]; and injecting a time delay between the first and second pulse of current [col. 6, lines 35-55]. Applicant's Admitted Prior Art further teaches that each memory has a controller comprising a write state machine [paragraph 2].

7. Claims 2-7, 9-14 and 16-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,793,694 to Akiba et al., in view of Applicant's Admitted Prior Art, and in further view of U.S. Patent 6,075,741 to Ma et al.

8. As to claim 2, Akiba discloses a system comprising a first memory [42a] and a second memory [42b]; a pulse generator [86] operable to generate a first current draw waveform of current to the first memory and a second current draw waveform of current to the second memory [col. 1, lines 61-67, col. 2, lines 1-16, and col. 6, lines 42-55]; and a delay circuit [88] operable to inject a time delay between the first and second current draw waveform of current [col. 6, lines 35-55], wherein the time delay is less than a duration of the current draw waveform applied to the first memory [FIG. 14]. Applicant's Admitted Prior Art further teaches that each memory has a controller comprising a write state machine [paragraph 2].

Akiba and Applicant's Admitted Prior Art teach the limitations of the claim, but does not teach that the pulse generator generates a plurality of pulses of current having a predetermined waveform.

Ma teaches that a system comprising a first memory [48] and a second memory [50]; a pulse generator [40] operable to generate a first current draw waveform of current to the first memory and a second current draw waveform of current to the second memory [col. 2, lines 35-44]; and a delay circuit [42] operable to inject a time delay between the first and second current draw waveform of current [col. 2, lines 45-48]. Thus, Ma teaches a pulse generator for a first and second memory similar to that of Akiba and Applicant's Admitted Prior Art. Ma further teaches the pulse generator generates a plurality of current draw waveform of current having a predetermined waveform [col. 5, lines 39-46]. In addition, Applicant's Admitted Prior Art further teaches that the waveform is associated with the operation of the memory, and has a large initial pulse of current followed by a subsequent plurality of smaller pulses of current [paragraph 2].

At the time that the invention was made, it would have been obvious to a person of ordinary skill in the art to employ the plurality of pulses of current as taught by Ma. One of ordinary skill in the art would have been motivated to do so that the memories would receive the proper amount of current.

It would have been obvious to one of ordinary skill in the art to combine the teachings of the cited references because they are both directed to the problem of initializing power to a plurality of memories in an electronic system. Moreover, the plurality of pulses of current means

taught by Ma would improve the operation of Akiba and Applicant's Admitted Prior Art because it allowed by preventing heat damage caused by high power dissipation [col. 1, lines 19-29].

9. As to claim 3, Ma discloses the delay circuit delays the second current draw waveform of current for at least as long as the duration of the large initial current draw waveform of current [col. 6, lines 22-31].

10. As to claim 4, Ma discloses the large initial pulse of the second current draw waveform of current occurs during a delay between the large initial pulse of current applied to the first write state machine and the plurality of subsequent pulses of current applied to the second write state machine [col. 6, lines 9-21].

11. As to claim 5, Ma discloses the large initial pulse of the second current draw waveform of current occurs during the delay between a first plurality of subsequent pulses applied to the first state machine and the plurality of subsequent pulses of current applied to the second write state machine [col. 6, lines 9-21].

12. As to claim 6, Ma discloses the first large initial pulse of current has an amplitude substantially equal to the amplitude of the second large initial pulse of current [col. 6, lines 60-67, and col. 7, lines 1-19].

13. As to claim 7, Ma discloses the pulse generator generates a plurality of pulses of current having a predetermined waveform [col. 5, lines 39-46]. Applicant's Admitted Prior Art further teaches that the waveform is associated with the operation of the memory, and has a large initial pulse of current followed by a subsequent plurality of smaller pulses of current [paragraph 2]. Furthermore, Applicant's Admitted Prior Art describes that the waveform may be of any well known to one of ordinary skill in the art [paragraph 19], such as wherein the plurality of additional pulses of current have amplitudes that are less than or equal to half of the amplitude of the first pulse of current.

14. As to claim 9, Ma discloses the pulse generator generates a plurality of pulses of current having a predetermined waveform [col. 5, lines 39-46]. Applicant's Admitted Prior Art further teaches that the waveform is associated with the operation of the memory, and has a large initial pulse of current followed by a subsequent plurality of smaller pulses of current [paragraph 2].

15. As to claim 10, Ma discloses the first pulse of current has an amplitude substantially equal to the amplitude of the second pulse of current [col. 6, lines 60-67, and col. 7, lines 1-19].

16. As to claim 11, Ma discloses the second current draw waveform of current occurs during a delay between the first initial current draw waveform of current applied to the first write state machine and the plurality of subsequent pulses of current applied to the second write state machine [col. 6, lines 9-21].

17. As to claim 12, Ma discloses the second pulse of current occurs during the delay between a first plurality of subsequent pulses applied to the first state machine and the plurality of subsequent pulses of current applied to the second write state machine [col. 6, lines 9-21].

18. As to claim 13, Ma discloses the delay circuit delays the second current draw waveform of current for at least as long as the duration of the first initial pulse of current [col. 6, lines 22-31].

19. As to claim 14, Ma discloses the pulse generator generates a plurality of pulses of current having a predetermined waveform [col. 5, lines 39-46]. Applicant's Admitted Prior Art further teaches that the waveform is associated with the operation of the memory, and has a large initial pulse of current followed by a subsequent plurality of smaller pulses of current [paragraph 2]. Furthermore, Applicant's Admitted Prior Art describes that the waveform may be of any well known to one of ordinary skill in the art [paragraph 19], such as wherein the plurality of additional pulses of current have amplitudes that are less than or equal to half of the amplitude of the first pulse of current.

20. As to claim 16, Ma discloses the pulse generator generates a plurality of pulses of current having a predetermined waveform [col. 5, lines 39-46]. Applicant's Admitted Prior Art further teaches that the waveform is associated with the operation of the memory, and has a large initial pulse of current followed by a subsequent plurality of smaller pulses of current [paragraph 2].

21. As to claim 17, Ma discloses the first pulse of current has an amplitude substantially equal to the amplitude of the second pulse of current [col. 6, lines 60-67, and col. 7, lines 1-19].

22. As to claim 18, Ma discloses the delay circuit delays the second pulse of current for at least as long as the duration of the first initial pulse of current [col. 6, lines 22-31].

23. As to claim 19, Ma discloses the second pulse of current occurs during a delay between the first initial pulse of current applied to the first write state machine and the plurality of subsequent pulses of current applied to the second write state machine [col. 6, lines 9-21].

24. As to claim 20, Ma discloses the second pulse of current occurs during the delay between a first plurality of subsequent pulses applied to the first state machine and the plurality of subsequent pulses of current applied to the second write state machine [col. 6, lines 9-21].

25. As to claim 21, Ma discloses the pulse generator generates a plurality of pulses of current having a predetermined waveform [col. 5, lines 39-46]. Applicant's Admitted Prior Art further teaches that the waveform is associated with the operation of the memory, and has a large initial pulse of current followed by a subsequent plurality of smaller pulses of current [paragraph 2]. Furthermore, Applicant's Admitted Prior Art describes that the waveform may be of any well known to one of ordinary skill in the art [paragraph 19], such as wherein the plurality of additional pulses of current have amplitudes that are less than or equal to half of the amplitude of the first pulse of current.

Response to Arguments

26. Applicant's arguments with respect to claims 1-21 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

27. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

28. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Chang whose telephone number is (571) 272-3671. The examiner can normally be reached on M-F 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on (571) 272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

December 8, 2006
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James K. Trujillo
JAMES K. TRUJILLO
PRIMARY EXAMINER
TC 2100